PRO-LOG
CORPORATION

STD 7000

7705A
32K EPROM
Memory Card

USER'S MANUAL

6/82

FOREWORD

This manual explains how to use Pro-Log's 7705A 32K EPROM Memory Card. It is structured to reflect the answers to basic questions that you, the user, might ask yourself about the 7705A. We welcome your suggestions on how we can improve our instructions.

The 7705A is part of Pro-Log's Series 7000 STD BUS hardware. Our products are modular, and they are designed and built with second-sourced parts that are industry standards. They provide the industrial manager with the means of utilizing his own people to control the design, production, and maintenance of the company's products that use STD BUS hardware.

Pro-Log supports its products with thorough and complete documentation. Also, to provide maximum assistance to the user, we teach courses on how to design with, and to use, microprocessors and the STD BUS products.

You may find the following Pro-Log documents useful in your work: *Microprocessor User's Guide* and the *Series 7000 STD BUS Technical Manual.* If you would like a copy of these documents, please submit your request on your company letterhead.

Contents

	Page
Foreword	ii
Figures	iv
Section 1-Purpose and Main Features	1-1
Section 2-Installation and Specifications	2-1
Installation	2-1
Address Mapping	2-3
MEMEX	2-6
Segment Select	2-7
Mechanical Specifications	2-7
Timing Diagrams	2-9
Section 3 - Operation and Programming	3-1
Introduction	3-1
MEMEX Example	3-1
MEMEX Control Software	3-1
MEMEX Control Software Example One	3-1
MEMEX Control Software Example Two	3-3
MEMEX Control Software Example Three	3-4
MEMEX Control Software Example Four	3-6
MEMEX Interrupt Control Software	3-9
Segment Select	3-12
Segment Select Control Software	3-16
Section 4—Operating Software	4-1
Section 5 - Maintenance	5-1
Reference Drawings	5-1
Operational Overview	5-4
Return for Repair Procedures	5-8
Limited Warranty	5-8

Figures

Figure		Page
1-1	7705A 32K EPROM Memory Card	1-1
1-2	Block Diagram of 7705A 32K EPROM Memory Card	1-2
2-1	7705A Installation	2-1
2-2	7705A Segment Select Connector	2-2
2-3	7705A Physical Locations of Features	2-3
2-4	7705A Socket Disable Jumper Table	2-4
2-5	7705A Memory Mapping Options	2-5
2-6	7705A Card Addressing Table	2-5
2-7	7705A Socket Address Table	2-6
2-8	7705A EDGE Connector Pin List	2-7
2-9	Electrical and Environmental Specifications — 7705A 32K ROM Card	2-8
2-10	Electrical Characteristics — 7705A 32K ROM Card	2-8
2-11	7705A Segment Connector Pin List	2-8
2-12	7705A Address Access Time	2-9
2-13	7705A RD* Access Time	2-10
2-14	7705A MEMEX Timing	2-10
2-15	7705A MEMRQ* Timing	2-11
2-16	7705A Segment Timing	2-11
3-1	MEMEX Example Using 7705A	3-2
3-2	MEMEX Software Example One for 7705A	3-3
3-3	MEMEX Software Example Two for 7705A	3-4
3-4	MEMEX Software Example Three for 7705A	3-5
3-5	Running MEMEX Software Example Three with 7705A	3-6
3-6	MEMEX Software Example Four for 7705A	3-7
3-7	Running MEMEX Software Example Four with 7705A	3-8
3-8	MEMEX Interrupt Software Flowchart for 7705A	3-10
3-9	MEMEX Interrupt Software Primary Memory for 7705A	3-11
3-10	MEMEX Interrupt Software Expanded Memory for 7705A	3-11
3-11	Segment Select Example One for 7705A	3-12
3-12	Segment Select Example Two for 7705A	3-13
3-13	MEMEX and Segment Select Example for 7705A	3-15
3-14	Segment Control Software with 7705A	3-16
5-1	Schematic for 7705A 32K EPROM Memory Card	5-2
5-2	Assembly Drawing for 7705A 32K EPROM Memory Card	5-3
5-3	Address Decoding Circuit for 7705A	5-4
5-4	Chip Enables Circuit for 7705A	5-5
5-5	ROM Output Enable for 7705A	5-6
5-6	Data Bus Buffer Circuit for 7705A	5-7

SECTION 1
Purpose and Main Features

Purpose

The 7705A card provides eight sockets for 2732/2732A EPROMS, for a total of 32K bytes of memory. The memory resides in one continuous block which can be mapped to either the upper or lower half of a 64K memory system.

It can respond to the STD BUS MEMEX line allowing two cards to reside in the same address field. A system using three 7705A cards and a Pro-Log processor card capable of controlling MEMEX can have greater than 64K bytes of memory with no additional cards or signal lines.

The 7705A card can also respond to an external Segment Select line, allowing it to participate in large-scale bank select schemes. The Segment Select line can be controlled by a memory segment controller or by I/O ports. One output port can control eight memory banks. Also, the 7705A can be tailored to fit small scale applications. Unused sockets can be disabled, allowing the card to occupy as little as 4K bytes of memory space which can be mapped anywhere within a 64K byte memory system.

Features

- **Eight 2732/A EPROM sockets — 32K byte capacity**
- **User-selectable memory mapping**
- **No wasted memory space - unused sockets can be disabled**
- **Responds to STD BUS MEMEX line**
- **Responds to external Segment Select line**
- **Processor independent — use with 8085, Z80, 6800, 8088, and others**

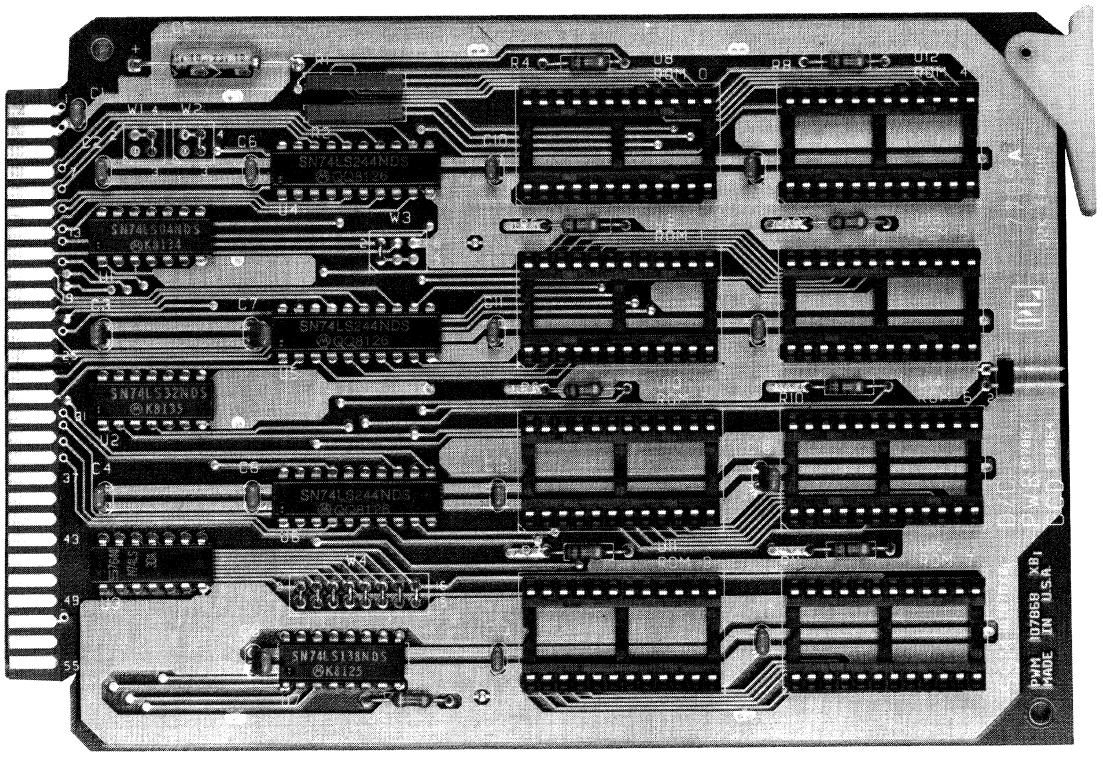


Figure 1-1. 7705A 32K EPROM Memory Card.

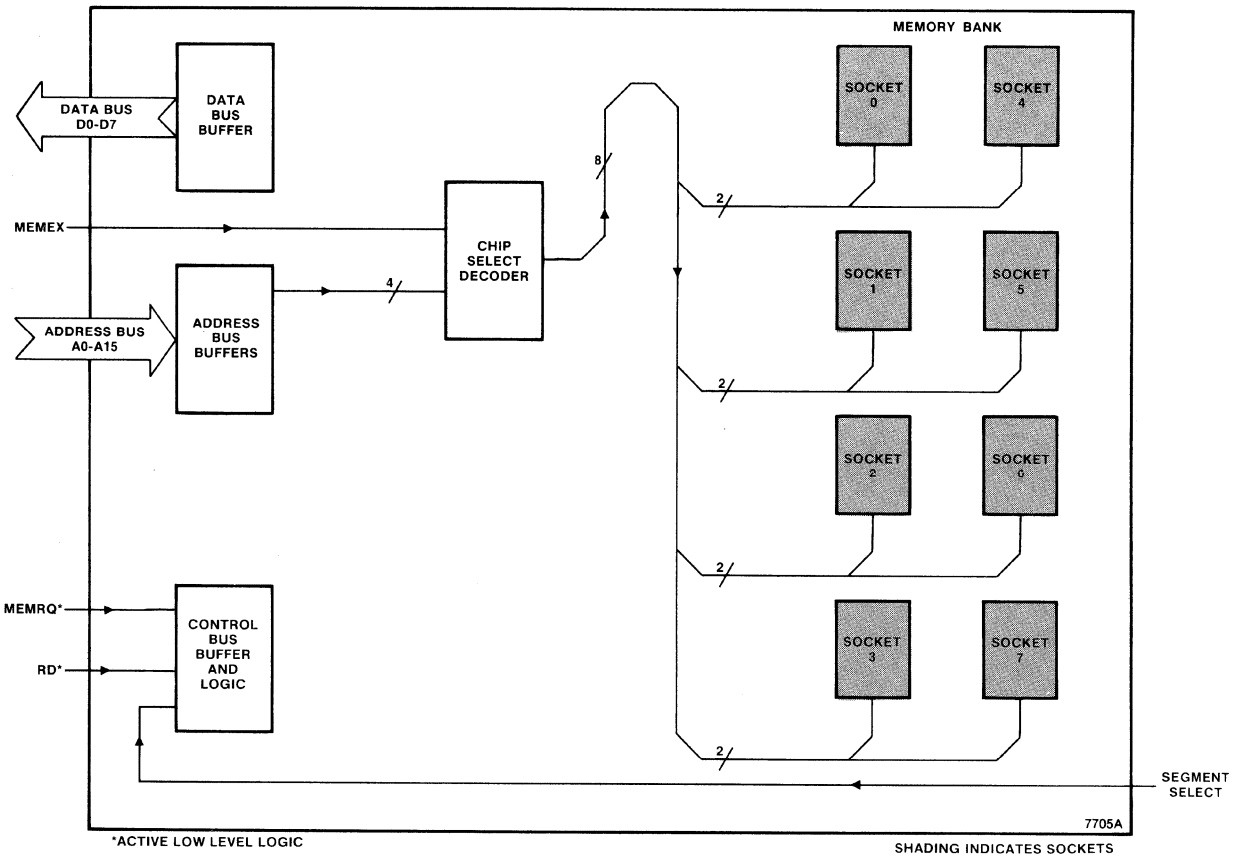


Figure 1-2. Block Diagram of 7705A 32K EPROM Memory Card.

SECTION 2
Installation and Specifications

Installation

The 7705A operates as part of an STD BUS card rack system. You can plug it directly into the STD BUS backplane, as shown in Figure 2-1, or extend it from the motherboard with a 7901 card extender. To use the 7901 card extender, plug it into any slot in the card rack and plug the 7705A into the connector on the 7901 card. This makes the 7705A accessible for testing.

> **CAUTION**
>
> To prevent possible damage to your STD BUS system make sure that power is off before inserting a card into the card rack, or before removing a card from the card rack.

The 7705A can occupy any slot in the card cage. It should be installed with the card ejector towards the top of the card rack as shown in Fig. 2-1.

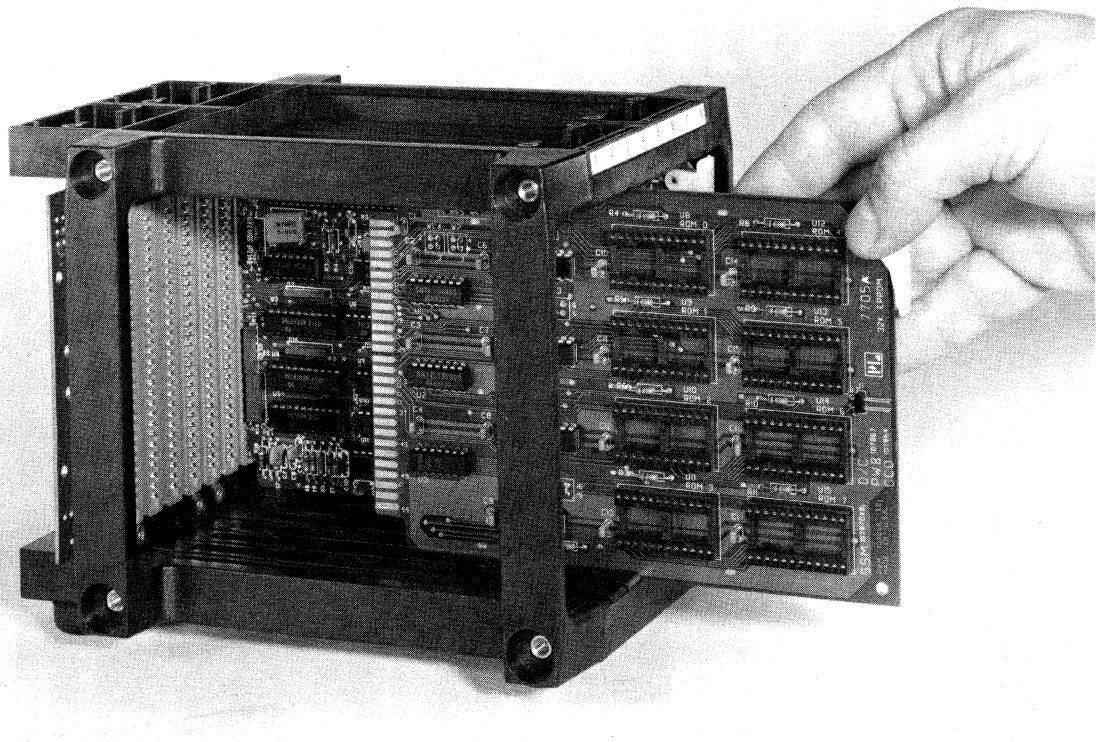


Figure 2-1. 7705A Installation

If the external Segment Select line is used, it should be attached as shown in Fig. 2-2. The connector type is a 2-pin 0.1-inch center connector. The cable should be a twisted pair, consisting of one signal line and one ground line for added noise immunity. The Pro-Log RC704 cable can be used for this purpose and can connect the 7705A card to an I/O card such as Pro-Log's 7605 card.

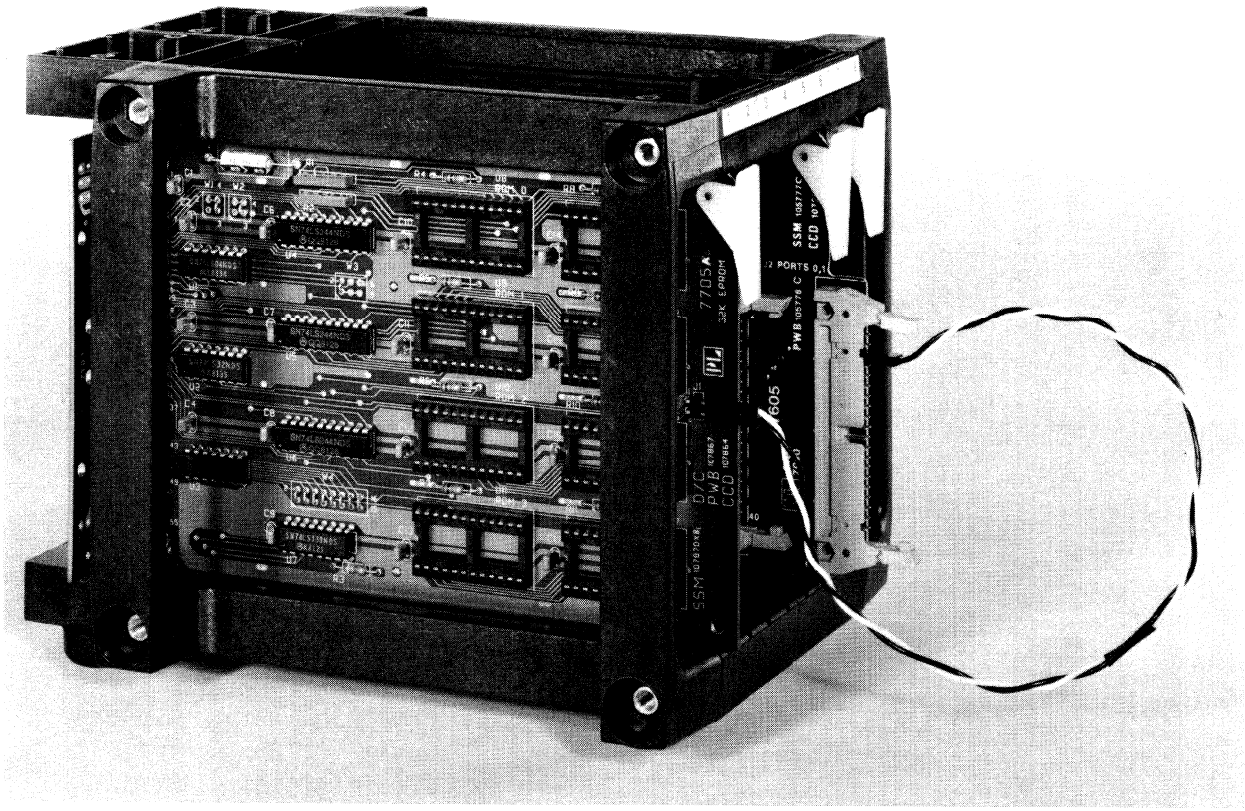


Figure 2-2. 7705A Segment Select Connector

Address Mapping

The 7705A card occupies 32K bytes of memory space. It decodes 16 address lines and can reside in either the upper or lower half of a 64K memory system.

As shipped from the factory, it occupies memory addresses 8000-FFFF. By way of jumper W1, shown in Fig. 2-3, its address mapping can be changed so that it occupies memory address 0000-7FFF. To change the addressing, remove jumper W1 from position 3-4 and replace it with one at position 1-2.

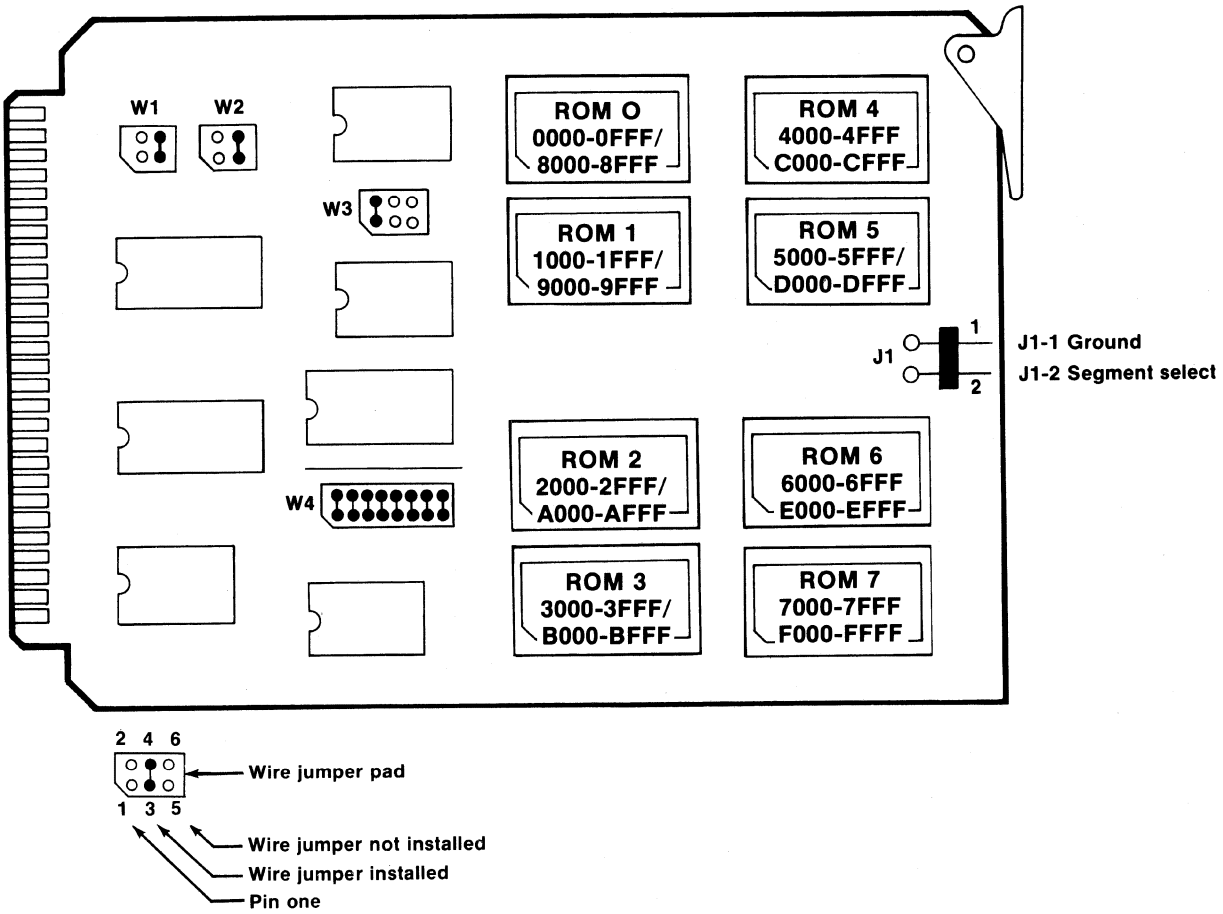


Figure 2-3. 7705A Physical Locations of Features

If less than the full 32K bytes of memory are used, the unused sockets can be disabled by removing the proper wire jumpers (Fig. 2-3). Jumper W4, positions 1-2 through 15-16 correspond to sockets 0-7 respectively. The location of these jumpers is shown in Figure 2-3. Figure 2-4 lists which socket is associated with each jumper in jumper pad W4. Figure 2-5 shows some of the possible combinations that a user can attain by moving W1 and W2 to various positions.

Figure 2-6 describes the address range the card is capable of occupying by moving Jumper W1 to its possible locations.

Figure 2-7 describes the addresses that each of the sockets is capable of occupying depending on the location of W1.

When a socket is disabled, chip select is disconnected from that socket. Also, memory on other cards in the system can occupy this address space without interference from the 7705A card. For a full description of how this works see Section 5, Maintenance under the "Chip Enable" heading.

Any number and combination of sockets may be disabled. By this method, the 7705A card can be configured to occupy as little as 4K of memory.

JUMPER	SOCKET
W4-1,2	0
W4-3,4	1
W4-5,6	2
W4-7,8	3
W4-9,10	4
W4-11,12	5
W4-13,14	6
W4-15,16	7

Figure 2-4. 7705A Socket Disable Jumper Table

ADDRESS RANGE	JUMPERS INSTALLED										COMMENTS
	W1 POSITION		W4 POSITION								
	1-2	3-4	1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16	
0000-0FFF	•		•								There are over 500 possible combinations. These are a few of the most commonly used configurations, and a few examples of how the 7705A can be used in situations requiring extreme flexibility.
0000-1FFF	•		•	•							
0000-2FFF	•		•	•	•						
0000-3FFF	•		•	•	•	•					
0000-4FFF	•		•	•	•	•	•				
0000-5FFF	•		•	•	•	•	•	•			
0000-6FFF	•		•	•	•	•	•	•	•		
0000-7FFF	•		•	•	•	•	•	•	•	•	
8000-8FFF		•	•								
8000-9FFF		•	•	•							
8000-AFFF		•	•	•	•						
8000-BFFF		•	•	•	•	•					
8000-CFFF		•	•	•	•	•	•				
8000-DFFF		•	•	•	•	•	•	•			
8000-EFFF		•	•	•	•	•	•	•	•		
8000-FFFF		•	•	•	•	•	•	•	•	•	Standard configuration (As shipped)
3000-3FFF	•					•					Example of how minimum 4K can be mapped anywhere.
F000-FFFF		•								•	For 6800 series start-up program or for bootstrap.
0000-0FFF/ 7000-7FFF	•		•							•	Example of noncontinuous memory mapping.

Symbol • means jumper installed.

Figure 2-5. 7705A Memory Mapping Options.

CONFIG.*	A15	ADDRESS RANGE	JUMPER W1-1,2	JUMPER W1-3,4
0	low	0000-7FFF	Installed	Open
1	high	8000-FFFF	Open	Installed

*Shipped in Configuration 1.

Figure 2-6. 7705A Card Addressing Table.

A14	A13	A12	ROM SOCKET	ADDRESS RANGE WITH JUMPER W1-1,2 INSTALLED	ADDRESS RANGE WITH JUMPER W1-3,4 INSTALLED
0	0	0	0	0000-0FFF	8000-8FFF
0	0	1	1	1000-1FFF	9000-9FFF
0	1	0	2	2000-2FFF	A000-AFFF
0	1	1	3	3000-3FFF	B000-BFFF
1	0	0	4	4000-4FFF	C000-CFFF
1	0	1	5	5000-5FFF	D000-DFFF
1	1	0	6	6000-6FFF	E000-EFFF
1	1	1	7	7000-7FFF	F000-FFFF

Figure 2-7. 7705A Socket Address Table.

MEMEX

This section explains the jumper options affecting MEMEX. The function and operation of the MEMEX line will be explained in Section 3.

As shipped, the 7705A card is enabled when MEMEX is low.To reverse its polarity, remove jumper W3 from position 1-2 and replace it with one at position 3-4. The location of this jumper is shown in Figure 2-3. When using two of these cards which are both going to occupy the same address field, one should have its polarity changed.

It is important to ensure that the MEMEX line is not left floating. The line must be either controlled by some other card in the system, or tied to ground on the 7705A itself. Pro-Log processor cards either control the MEMEX line or simply tie it to ground. If there is no card in the system controlling MEMEX, or if you want the card to disregard MEMEX, jumper W3 can be removed from the position 3-4 or 1-2 and be replaced by one at position 5-6. This will tie the line to ground and permanently enable the card.

Segment Select.

This section explains the jumper options affecting Segment Select. The function and operation of the Segment Select line will be explained in Section 3.

The Segment Select line is not a part of the STD BUS. It is an external line which must be connected on the card ejector side of the 7705A, when it is used. Figure 2-3 shows the location of the connector.

The connector type is a 2-pin, 0.1-inch center connector. The cable should be a twisted pair, consisting of one signal line and one ground line for added noise immunity. Figure 2-3 shows which pin is signal and which is ground.

An I/O card, such as Pro-Log's 7605 card, along with an RC704 cable can be used to control the line. One output bit or line per segment is required. Therefore, one output port can control eight segments or memory banks.

As shipped the card is enabled when the Segment Select line is in the high state. Its polarity can be reversed by removing jumper W2 from position 3-4 and replacing it with one at position 1-2. (See Fig. 2-3).

With jumper W2 in position 3-4 the Segment Select line can be left unconnected. A pull-up resistor on the line will hold it in the active condition. If jumper W2 is in position 1-2 however, the line must be controlled in some manner, or the card will remain permanently disabled.

STD BUS Edge Connector Pin List

Figure 2-8 describes the signals found on the 7705A Edge Connector. It also describes the LSTTL load/drive capability of the 7705A. Figure 2-9 describes the Electrical and Environmental Specifications for the 7705A. Figure

2-10 describes the Electrical Characteristics of the 7705A. Figure 2-11 describes the pinout and LSTTL load of the Segment Select connector.

Mechanical Specifications

The 7705A meets all general mechanical specifications of the STD BUS.

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
+5V	Vcc		2	1		Vcc	+5V
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7		55	8	7	55		D3
D6		55	10	9	55		D2
D5		55	12	11	55		D1
D4		55	14	13	55		D0
A15	2		16	15		1	A7
A14	1		18	17		1	A6
A13	1		20	19		1	A5
A12	1		22	21		1	A4
A11	1		24	23		1	A3
A10	1		26	25		1	A2
A9	1		28	27		1	A1
A8	1		30	29		1	A0
RD*	1		32	31			WR*
MEMRQ*	1		34	33			IORQ*
MEMEX[1]	1		36	35			IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47			SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

* Active low-level logic
[1] Selectable logic polarity

Figure 2-8. 7705A Edge Connector Pin List.

MNEM.	Recommended Operating Limits				Absolute Non-Operating Limits		
	PARAMETER	MIN	TYP	MAX	MIN	MAX	UNITS
V_{CC}	Supply Voltage	4.75	5.00	5.25	0	5.50	Volts
—	Free Air Temperature	0	+25	+55	-40	+75	°C
—	Humidity	5	—	95[1]	5	95[1]	%RM

[1]Non-condensing

Figure 2-9. Electrical and Environmental Specifications—7705A 32K ROM CARD.

MNEM.	PARAMETER	MIN	TYP	MAX	UNITS
ICC	VCC Supply Current	—	300	600	milliAmps*

***NOTE:** Assumes all memory sockets loaded with one selected and seven in standby. For unused 2732A sockets, subtract 150mA maximum selected or 30mA maximum in standby.

Figure 2-10. Electrical Characteristics—7705A 32K ROM CARD.

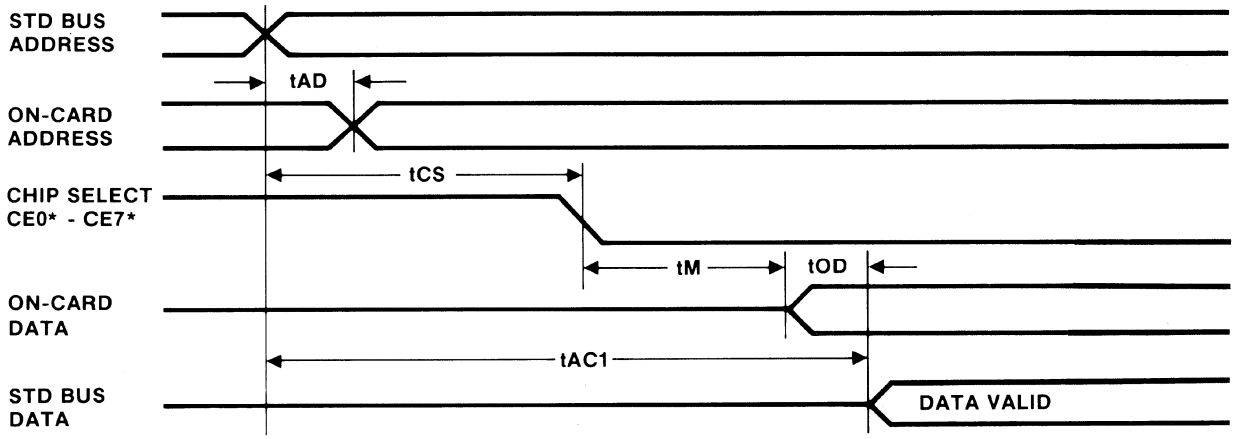
PIN NUMBER			PIN NUMBER	
INPUT (LSTTL DRIVE)				
MNEMONIC				MNEMONIC
SEGMENT[1]	5	2	1	GROUND

[1] Selectable logic polarity

Figure 2-11. 7705A Segment Connector Pin List.

Timing Specifications

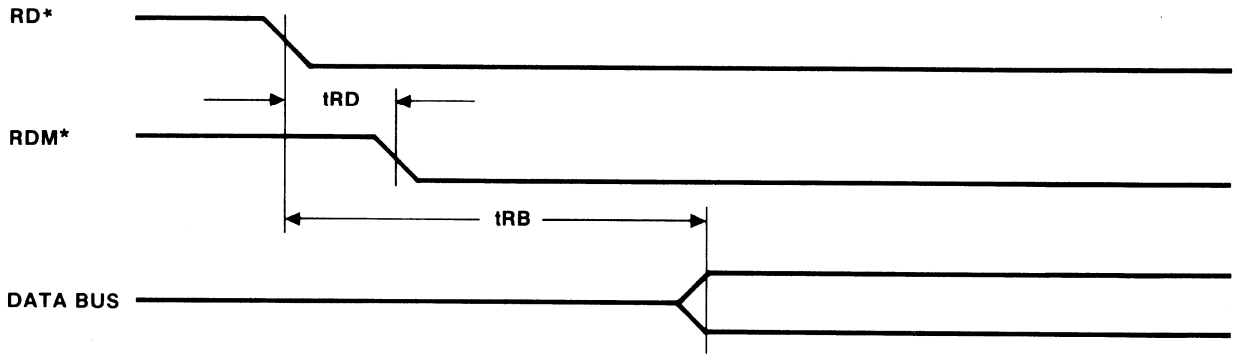
Figures 2-12 through 2-16 describe the various timing specifications affecting the 7705A.



SYMBOL	PARAMETER	NANOSECONDS		
		MIN	TYP	MAX
tAC	Minimum safe access time for read	175	—	—
tAD	Address buffer time delay	—	15	30
tCS	Chip select logic time	—	35	60
tOD	Data bus buffer time delay	—	15	30
tM	Data buffer enable time	—	60	100

All above times are assuming that RD*, MEMRQ*, MEMEX, and SEGMENT* are active prior to STD BUS address becoming valid.

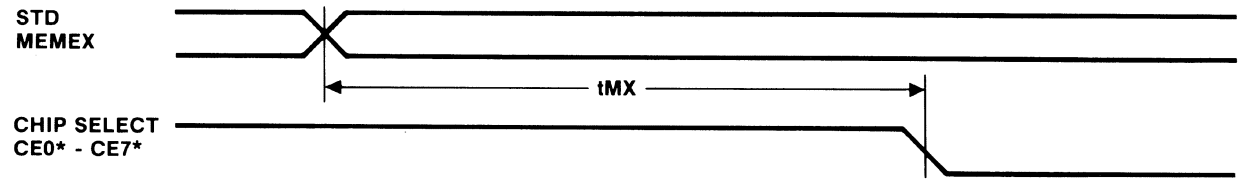
Figure 2-12. 7705A Address Access Time.



SYMBOL	PARAMETER	NANOSECONDS	
		TYP	MAX
tRD	Time RD* till RDM*	25	50
tRB	Time RD* till data bus buffer enabled	0	100

RD can go active up to 115 nseconds after MEMRQ and up to 125 nseconds after address valid without affecting access time. If RD* comes later the time should be added to the minimum access time of the card. Normally RD* goes true during the memory device access time and therefore does not affect access time for the card.

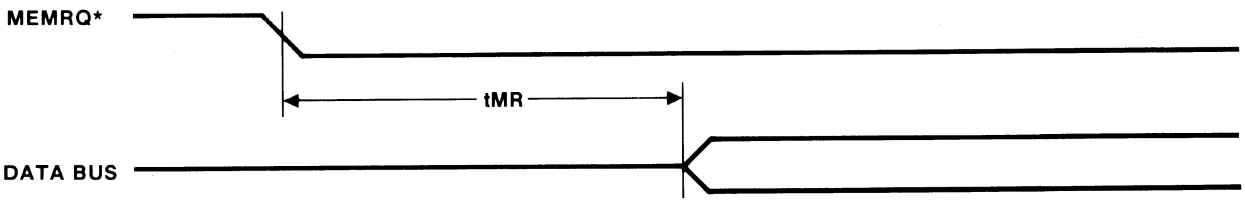
Figure 2-13. 7705A RD* Access Time.



SYMBOL	PARAMETER	NANOSECONDS	
		TYP	MAX
tMX	Time MEMEX active to chip select* active	45	75

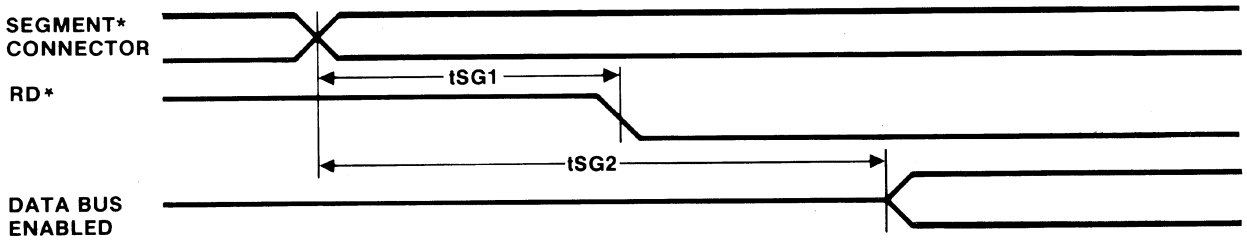
The above parameter is true if all other signals are active prior to MEMEX going active.

Figure 2-14. 7705A MEMEX Timing



SYMBOL	PARAMETER	NANOSECONDS	
		TYP	MAX
tMR	MEMRQ* active till data bus buffer enabled	—	100

Figure 2-15. 7705A MEMRQ* Timing



SYMBOL	PARAMETER	NANOSECONDS	
		TYP	MAX
tSG1	SEGMENT active to RD*	40	65
tSG2	SEGMENT active to data bus driver enabled	70	120

The above parameters are true if all other signals are active prior to SEGMENT* going active.

Figure 2-16. 7705A Segment Timing.

SECTION 3
Operation and Programming

Introduction

This section explains the function and use of the 7705A card. The card is designed to be a versatile part of your memory system.

It can be used in both small and large-scale applications. By using the memory size and mapping options described in Section 2, and the MEMEX and Segment Select lines described in this section, the 7705A can fill the ROM memory requirements of virtually any system.

MEMEX

The MEMEX line is part of the STD BUS. It is used as a memory bank select line. Using this line allows two banks of memory to occupy the same address field. Only one of the banks is selected at a time, depending on the logic state of the MEMEX line.

It is normally controlled by a memory segment controller, or an output port.

The segment controller or output port can be either on the processor card or on some other card in the system. Some Pro-Log processor cards have an onboard output port for controlling MEMEX.

MEMEX Example

An example of how MEMEX can be used is shown in Fig. 3-1, MEMEX Example. It shows a 124K memory system. It is comprised of 4K of RAM and 120K of ROM. The RAM is on the processor card and is permanently enabled. That is, it ignores MEMEX. The ROM is in two 60K banks. Each bank consists of two 7705A cards. Only two cards are enabled at a time: the two on the left when MEMEX is low and the two on the right when it is high. (See Fig. 3-1).

MEMEX Control Software

The software for controlling MEMEX requires some special consideration. Care must be taken that the processor does not get confused when changing memory banks.

There are a number of ways to deal with this. What follows are a few examples.

MEMEX Control Software Example One

In many systems using MEMEX, it will be advantageous to keep some section of memory permanently enabled, thus creating a section which disregards MEMEX. This may be a section of ROM memory at the low order addresses, a section of RAM used to store registers, program variables, and the stack, or a section of ROM containing interrupt service that need to be quickly accessible at all times.

If your system will have a permanently enabled section of memory, the MEMEX Control software can reside in this section. If the section is ROM, the program would simply reside in the ROM. If the section is RAM the processor could load the program into the RAM. The program would be stored in ROM, disk, or some other nonvolatile memory. The processor would load the program into RAM as part of the power-up initialization process.

Using the system in Fig. 3-1 as a model, a program could be written like the one shown in Fig. 3-2. It assumes you are jumping from a main program in one bank to a subroutine in the other bank. The address of the subroutine you are jumping to must be in the H,L register pair. The program selects the proper memory bank and jumps to the subroutine. When the subroutine is exited the processor returns to the MEMEX control program. The program reselects the original bank then returns to the program from which it came.

Fig. 3-2 shows two programs. One to jump to a subroutine in Expanded memory and one to jump to a subroutine in Primary memory.

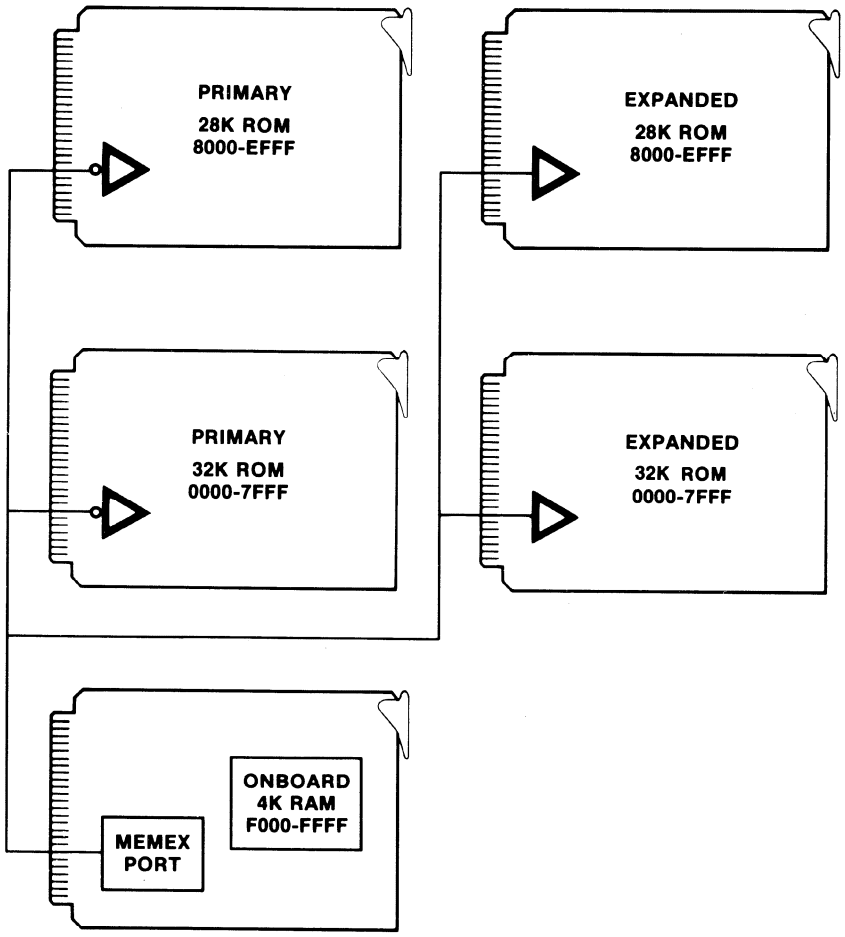


Figure 3-1. MEMEX Example using 7705A.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

TITLE MEMEX SOFTWARE EX. DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
FF	E 0	3E	(TO EXP.)	LDA	I	SET MEMEX HIGH, ENABLES
	1	01		—	01	EXPANDED MEMORY
	2	D3		OPA		
	3	XX		—	XX	← PORT ADDRESS
	4	E5		PSP	H,L	PUSH RETURN ADDRESS (FFEA)
	5	21		LDPI	H,L	ON TO STACK
	6	EA		—		
	7	EF		—		
	8	E3		XCPT	H,L	
	9	E9		JPN	(H,L)	JUMP TO SUBROTINE AT H,L
	A	3E		LDA	I	SET MEMEX LOW ENABLES
	B	00		—	00	PRIMARY MEMORY
	C	D3		OPA		
	D	XX		—	XX	← PORT ADDRESS
	E	C9		RTS		EXIT
	F					
	F 0	3E	(TO PRI.)	LDA	I	SET MEMEX LOW, ENABLES
	1	00		—		PRIMARY MEMORY
	2	D3		OPA		
	3	XX		—		← PORT ADDRESS
	4	E5		PSP	H,L	PUSH RETURN ADDRESS (FFFA)
	5	21		LDPI	H,L	ONTO STACK
	6	FA		—		
	7	EF		—		
	8	E3		XCPT	H,L	
	9	E9		JPN	(HL)	JUMP TO SUBROUTINE AT H,L
	A	3E		LDA	I	SET MEMEX HIGH, ENABLES
	B	01		—		EXPANDED MEMDRY
	C	D3		OPA		
	D	XX		—		← PORT ADDRESS
	E	C9		RTS		EXIT
	F					

PERMANENT MEMORY

100001 2/77

Figure 3-2. MEMEX Software Example One for 7705A.

MEMEX Control Software Example Two

In the first example it was assumed that any time the program jumped from one bank to the other it was to jump to a subroutine. Fig. 3-3 is a program for jumping from one bank to the other, not to a subroutine.

The program simply changes the state of the MEMEX line and then jumps to the address in the H,L register pair. Again, the program is divided up into two sections.One to go from Primary to Expanded memory, and one to do the opposite.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

TITLE MEMEX SOFTWARE EX. 2 DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
FF	F 0	3E	TO EXP.	LDA	I	PERMANENT MEMORY: SET MEMEX HIGH, SELECTS EXPANDED MEMORY
	1	01		—		
	2	D3		OPA		← PORT ADDRESS
	3	XX		—		
	4	F9		JPN	(H,L)	JUMP TO ADDRESS IN H,L PAIR
	5					
	6					
	7					
	8					
	9	3E	TOPRI.	LDA	I	SET MEMEX LOW, SELECTS PRIMARY MEMORY
	A	00		—		
	B	D3		OPA		← PORT ADDRESS
	C	XX		—		
	D	E9		JPN	(H,L)	JUMP TO ADDRESS IN H,L PAIR
	E					
	F					
	0					
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					

100001 2/77

Figure 3-3. MEMEX Software Example Two for 7705A.

MEMEX Control Software Example Three

So far we have looked at MEMEX control software residing in a section of memory which is permanently enabled. Figures 3-4 and 3-5 show how the control software can reside in memory that is affected by MEMEX.

Figure 3-4 shows how a program can be written to jump from a program in Primary Memory to a subroutine in Expanded memory. Note that both sections of the program reside at the same addresses. However, one part is in Primary memory and one part is in Expanded memory.

Figure 3-5 shows how the program looks to the processor. When it is run, it becomes one coherent program.

This program only allows for jumping from Primary memory to a subroutine in Expanded memory and then returning. In normal operation you would probably also want one to do the opposite.

To use the program shown in Fig. 3-5, you must be in Primary memory. When you want to jump to a subroutine in Expanded memory, you load the address of the subroutine into the H,L register pair. Then perform a Jump to Subroutine to the MEMEX control program. The program will direct the processor to change memory banks and jump to the subroutine. After running the subroutine, the processor will be returned to your original program.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

TITLE MEMEX SOFTWARE EX.3 DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
EF	F 0	3E		LDA	I	PRIMARY MEMORY — JUMP TO EXPANDED MEMORY
	1	01		—		
	2	D3		OPA		
	3	XX		—		← PORT ADDRESS
	4	00		NOP		UNUSED
	5	00		NOP		
	6	00		NOP		
	7	00		NOP		
	8	00		NOP		
	9	00		NOP		
	A	00		NOP		
	B	00		NOP		
	C	00		NOP		
	D	00		NOP		
	E	C9		RTS		EXIT
	F					
EF	F0	00		NOP		EXPANDED MEMORY — UNUSED
	1	00		NOP		
	2	00		NOP		
	3	00		NOP		
	4	E5		PSP	H,L	PUSH RETURN ADDRESS (EFFA)
	5	21		LDPI	H,L	ONTO STACK
	6	FA		—		
	7	EF		—		
	8	E3		XCPT	H,L	
	9	E9		JPN	(H,L)	JUMP TO SUBROUTINE AT H,L
	A	3E		LDA	I	JUMP TO PRIMARY MEMORY
	B	00		—	00	
	C	D3		OPA		
	D	XX		—		← PORT ADDRESS
	E	00		NOP		UNUSED
	F					

100001 2/77

Figure 3-4. MEMEX Software Example Three for 7705A.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

TITLE RUNNING EX.3 DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
EF	F0	3E		LDA	I	JUMP TO EXPANDED MEMORY
	1	01		—		
	2	D3		DPA		
	3	XX		—		← PORT ADDRESS
	4	E5		PSP	HL	PUSH RETURN ADDRESS (EFFA)
	5	21		LDPI	HL	ONTO STACK
	6	FA		—		
	7	EF		—		
	8	E3		XCPT	HL	
	9	E9		JPN	HL	JUMP TO SUBROUTINE AT H,L
	A	3E		LDA	I	JUMP TO PRIMARY MEMORY
	B	00		—	00	
	C	D3		OPA		
	D	XX		—		← PORT ADDRESS
	E	C9		RTS		EXIT
	F					
	0					
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					

100001 2/77

Figure 3-5. Running MEMEX Software Example Three with 7705A.

MEMEX Control Software Example Four

The example shown in Fig. 3-6 is similar to the last example. In this one however, rather than jumping from one bank to another as a subroutine, a simple jump is performed.

This program is in two sections: one to go from Primary to Expanded memory and one to do the opposite.

Figure 3-7 shows how the program looks to the processor.

To use the program, load the address of the program you want to jump to into the H,L register pair. Then, jump to the MEMEX control program. The processor is directed to change memory banks, then jump to the program you requested.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

TITLE MEMEX SOFTWARE Ex.4 DATE

HEXADECIMAL PAGE ADR.	HEXADECIMAL LINE ADR.	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER		COMMENTS
EF	F0	3E	TO EXP.	LDA	I	PRIMARY MEMORY	JUMP TO EXPANDED MEMORY
	1	01		—	01		
	2	D3		OPA			
	3	XX		—			← PORT ADDRESS
	4	00		NOP			UNUSED
	5						
	6						
	7						
	8	00	TO PRI.	NOP			
	9	00		NOP			UNUSED
	A	00		NOP			
	B	00		NOP			
	C	E9		JPN	HL		
	D						JUMP TO ADDRESS IN H,L
	E						
	F						
EF	F0	00	TO EXP.	NOP		EXPANDED MEMORY	UNUSED
	1	00		NOP			
	2	00		NOP			
	3	00		NOP			
	4	E9		JPN	HL		JUMP TO ADDRESS IN H,L
	5						
	6						
	7						
	8	3E	TO PRI.	LDA	I		JUMP TO PRIMARY MEMORY
	9	00		—	00		
	A	D3		OPA			
	B	XX		—			← PORT ADDRESS
	C	00		NOP			UNUSED
	D						
	E						
	F						

100001 2/77

Figure 3-6. MEMEX Software Example Four for 7705A.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

TITLE RUNNING EX.4 DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
EF	F 0	3E	TO EXP.	LDA	I	PRI.MEM: JUMP TO EXPANDED MEMORY
	1	01		—	01	
	2	D3		OPA		
	3	XX		—		← PORT ADDRESS
	4	E9		JPN	H,L	JUMP TO ADDRESS IN H,L
	5					EXP MEM
	6					
	7					
	8	3E	TO PRI.	LDA	I	JUMP TO PRIMARY MEMORY
	9	00		—	00	
	A	D3		OPA		
	B	XX		—		← PORT ADDRESS
	C	E9		JPN	H,L	PRI.MEM: JUMP TO ADDRESS IN H,L
	D					
	E					
	F					
	0					
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					

100001 2/77

Figure 3-7. Running MEMEX Software Example Four with 7705A.

MEMEX Interrupt Control Software

This last example shows how interrupt service can be handled in a system using MEMEX.

One method previously mentioned is to set aside an area of memory for interrupt service. This area would be permanently enabled.

A second method can be used if the interrupt service routines are short enough. This method has identical service routines in both Primary and Expanded memory. Both routines would reside at the same addresses. This method can, however, use up too much memory space.

A third method is shown in Fig. 3-8, 9, and 10. In this method, the service routines reside in only one bank of memory. In the example shown, they reside in Primary memory.

The function of the program is to coordinate the jumping to, and returning from, the interrupt routine. The program ensures that the processor gets to the service routine. If the processor is in Expanded memory, it directs it to switch to Primary memory. It also ensures that the processor returns to the correct bank, after the interrupt is serviced.

The routine resides at address 0024. This is the address an 8085 processor jumps to when it receives a non-maskable interrupt.

Follow the flowchart in Fig. 3-8 and assume that the processor is in expanded memory when it is interrupted. The program then directs the processor to select primary memory by clearing the MEMEX bit in the accumulator and writing it out to the MEMEX port. In primary memory, the processor complements and stores the MEMEX bit. After the interrupt is serviced, the MEMEX bit is retrieved. When the bit is output to the MEMEX port, the processor is first returned to expanded memory and then to the program from which it was interrupted.

If the processor is in primary memory when it is interrupted, it sets the MEMEX bit in the accumulator to a one. The one is then complemented and stored. After the interrupt is serviced, the MEMEX bit is retrieved and is output to the MEMEX port; this has no effect, however, since the MEMEX line is already low. The processor simply continues in primary memory. It then returns to the program from which it was interrupted.

Figures 3-9 and 3-10 show how this program could be written. The program in Figure 3-9 would reside in Primary memory and the program in Fig. 3-10, in Expanded memory. One of these programs should reside at each address where an interrupt service routine is located.

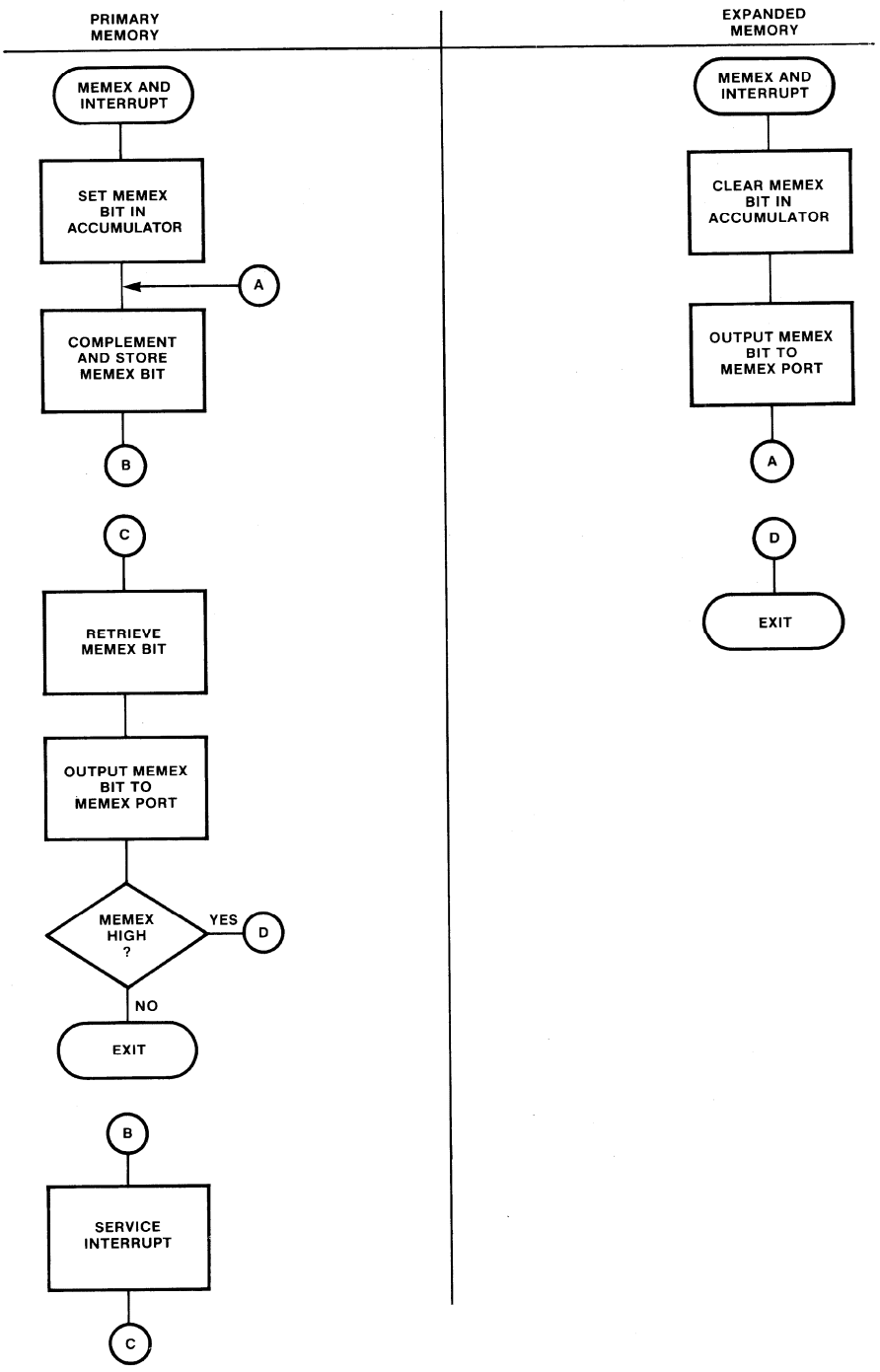


Figure 3-8. MEMEX, Interrupt Software Flowchart for 7705A.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

TITLE MEMEX + INTER — DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTR	MNEMONIC MODIFIER	COMMENTS
00	20					
	1					
	2					
	3					
	24	3E	(MEMEX + INTER.)	LDA	I	SET MEMEX BIT IN ACCUMULATOR
	5	01		—	01	
	6	00		NOP		
	7	00		NOP		
	8	2F		CMA		COMPLEMENT AND STORE
	9	F5		PSP	AF	MEMEX BIT
	A	C3		JP	UN	SKIP OVER "EXIT" TO "INTER"
	B	31		—		
	C	00		—	INTER	
	D	F1	EXIT	PLP	AF	RETRIEVE AND OUTPUT MEMEX BIT
	E	D3		OPA		
	F	XX		—		← PORT ADDRESS
	30	C9		RTS		EXIT (PRIMARY MEMORY)
	1	XX	INTER			INTERRUPT SERVICE
	2	XX				
	3	XX				
	4	XX				
	5	XX				
	6	XX				
	7	XX				
	8	XX				
	9	XX				
	A	XX				
	B	XX				
	C	XX				
	D	C3		JP	UN	GO EXIT
	E	2D		—		
	F	00		—	EXIT	

PRIMARY MEMORY

100001 2/77

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

TITLE MEMEX + INTER — DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR	MNEMONIC LABEL	MNEMONIC INSTR	MNEMONIC MODIFIER	COMMENTS
00	20					
	1					
	2					
	3					
	24	3E	(NEMEX + INTER)	LDA	I	CLEAR AND OUTPUT MEMEX BIT,
	5	00		—	00	SELECTS PRIMARY MEMORY
	6	D3		OPA		
	7	XX		—		← PORT ADDRESS
	8	00		NOP		UNUSED
	9	00		NOP		
	A	00		NOP		
	B	00		NOP		
	C	00		NOP		
	D	00		NOP		
	E	00		NOP		
	F	00		NOP		
	30	C9		RTS		EXIT (EXPANDED MEMORY)
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					

EXPANDED MEMORY

100001 2/77

Figure 3-10. MEMEX, Interrupt Software Expanded Memory for 7705A.

Segment Select

The Segment Select line is not a part of the STD BUS, but is an external line which must be connected on the card ejector side of the 7705A, when it is used. Figure 2-2 shows the location of the connector. The purpose of the line is to allow the 7705A card to participate in large scale memory bank select schemes, where multiple cards occupy the same address field.

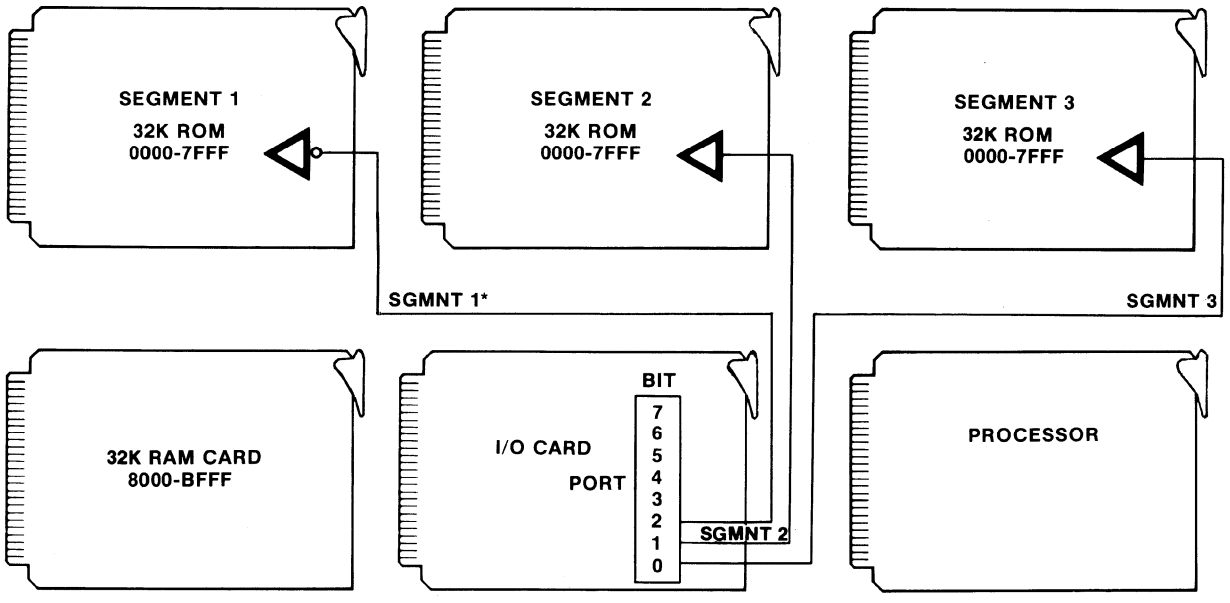
Whereas the MEMEX line can be used to select one of two banks of memory, the segment Select line can choose one of any number of memory banks.

The line is normally controlled by a memory segment controller or by output ports. An I/O card such as Pro-Log's 7605 card along with an RC704 cable can be used to control the line. One output port can control eight cards.

Figure 3-11 is an example of how the line can be used. It shows a 128K memory system with 32K RAM and 96K ROM. The 32K RAM is on a card which is permanently enabled. The 96K ROM is on three cards. Each card has its Segment Select line connected to a bit of an output port on an I/O card. All three cards occupy the same address field.

At power up, the output port bits would be low. One of the 7705A cards would be configured for low-level active Segment Select. The other two would be high level active. Therefore, one of the cards would automatically be selected at power up. The processor could thereafter choose which card it wanted simply by writing to the output port.

Another example is shown in Fig. 3-12. In this case there are two cards connected to each output line being used. There is 4K of RAM on the processor card which is permanently enabled and 180K of ROM in three banks. Each bank consists of two cards.



128K MEMORY SYSTEM
96K ROM
32K RAM

Figure 3-11. Segment Select Example One for 7705A.

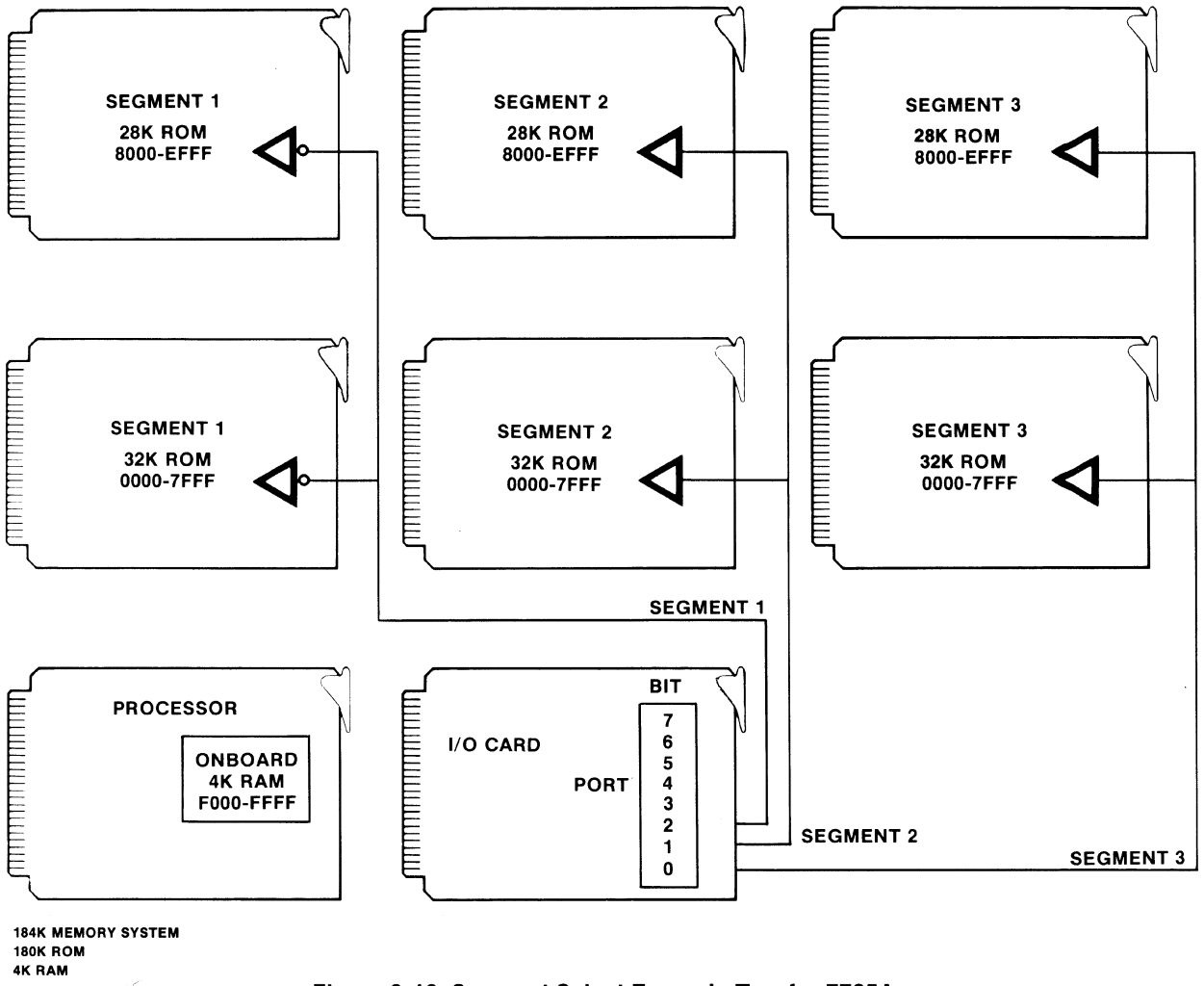


Figure 3-12. Segment Select Example Two for 7705A.

Finally, there is a third example combining MEMEX and Segment Select. MEMEX will be used normally, since it requires no additional lines. If Segment Select is used, MEMEX will probably not be used. However, they can be used together.

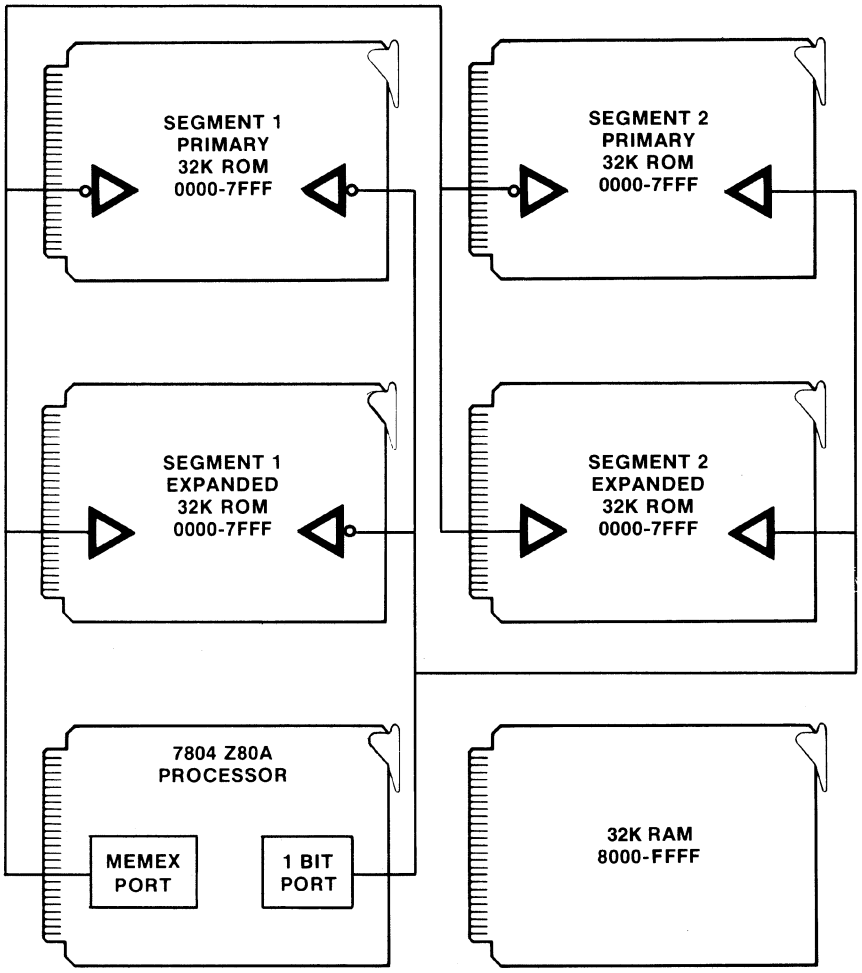
In Fig. 3-13, a 160K system is shown. It has 32K of RAM which is permanently enabled.The rest, 128K of ROM, is in four banks.

The processor card is a Pro-Log 7804 card. It has one output line which is used here for Segment Select.

This one Segment Select line is connected to all four ROM cards. The two marked Segment One are enabled when Segment Select is low. The two marked Segment Two are enabled when Segment Select is high.

The processor selects one segment, or pair, of cards by setting the Segment Select line high or low. It then selects which of the cards in the pair is enabled by setting the MEMEX line high or low.

Of the two cards marked Segment One, one is enabled when MEMEX is low, and one when it is high. The same is true for the cards marked Segment Two.



160K MEMORY SYSTEM
128K ROM
32K RAM

Figure 3-13. MEMEX and Segment Select Example for 7705A.

Segment Select Control Software

The control software for Segment Select is very similar to that used for MEMEX. The difference is that it must be able to control more than two Segments. To do this, the program must be told what Segment to jump to. It must also be told what Segment to return to.

As with MEMEX, many applications will require an area of Permanent memory. The simplest Segment Control software would reside in this area. Fig. 3-14 is an example of such a program.

It is similar to the program in MEMEX Software Example One. It coordinates jumping from one segment to a subroutine in another segment. The difference here is that you must enter the program with two additional variables. Register A must have the number of the segment you are jumping to. Register B must have the number of the segment you are jumping from.

The "number" of the segment would be 01, 02, 04, 08, 10, 20, 40, or 80 HEX. One bit for each segment. This program can therefore control up to eight segments.

Any of the MEMEX control software examples can be adapted for Segment Control. Or entirely different control software can be written. Use these as examples from which to write your own program.

PRO-LOG CORPORATION — PROGRAM ASSEMBLY FORM

TITLE SEGMENT CONTROL DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
FF	F0	D3		OPA		SWITCH TO DESIRED SEGMENT
	1	XX		—		— PORT ADDRESS
	2	C5		PSP	BC	SAVE ORIGINAL SEGMENT NUMBER
	3	E5		PSP	H,L	PUSH RETURN ADDRESS ON (FFF9)
	4	21		LDPI	H,L	TOP OF STACK
	5	F9		—		
	6	FF		—		
	7	E3		XCPT	H,L	
	8	E9		JPN	H,L	JUMP TO SUBROUTINE AT H,L
FF	F9	C1		PLP	B,C	RETURN TO ORIGINAL SEGMENT
	A	78		LDA	B	
	B	D3		OPA		
	C	XX		—		— PORT ADDRESS
	D	C9		RTS		EXIT
	E					
	F					
	0					
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					

PERMANENT MEMORY

100001 2/77

Figure 3-14. Segment Control Software with 7705A.

SECTION 4
Operating Software

Introduction

This section is usually reserved for operating software. However, the 7705A card requires no software except for those examples given in Section 3.

SECTION 5
Maintenance

Reference Drawings

The schematic (Figure 5-1) and assembly drawing (Figure 5-2) in the following pages are included in this manual FOR REFERENCE USE ONLY. They may differ in some respects from the card and documentation that the user receives from Pro-Log.

The schematic and the assembly drawing shipped by Pro-Log with the card are those from which the card was manufactured.

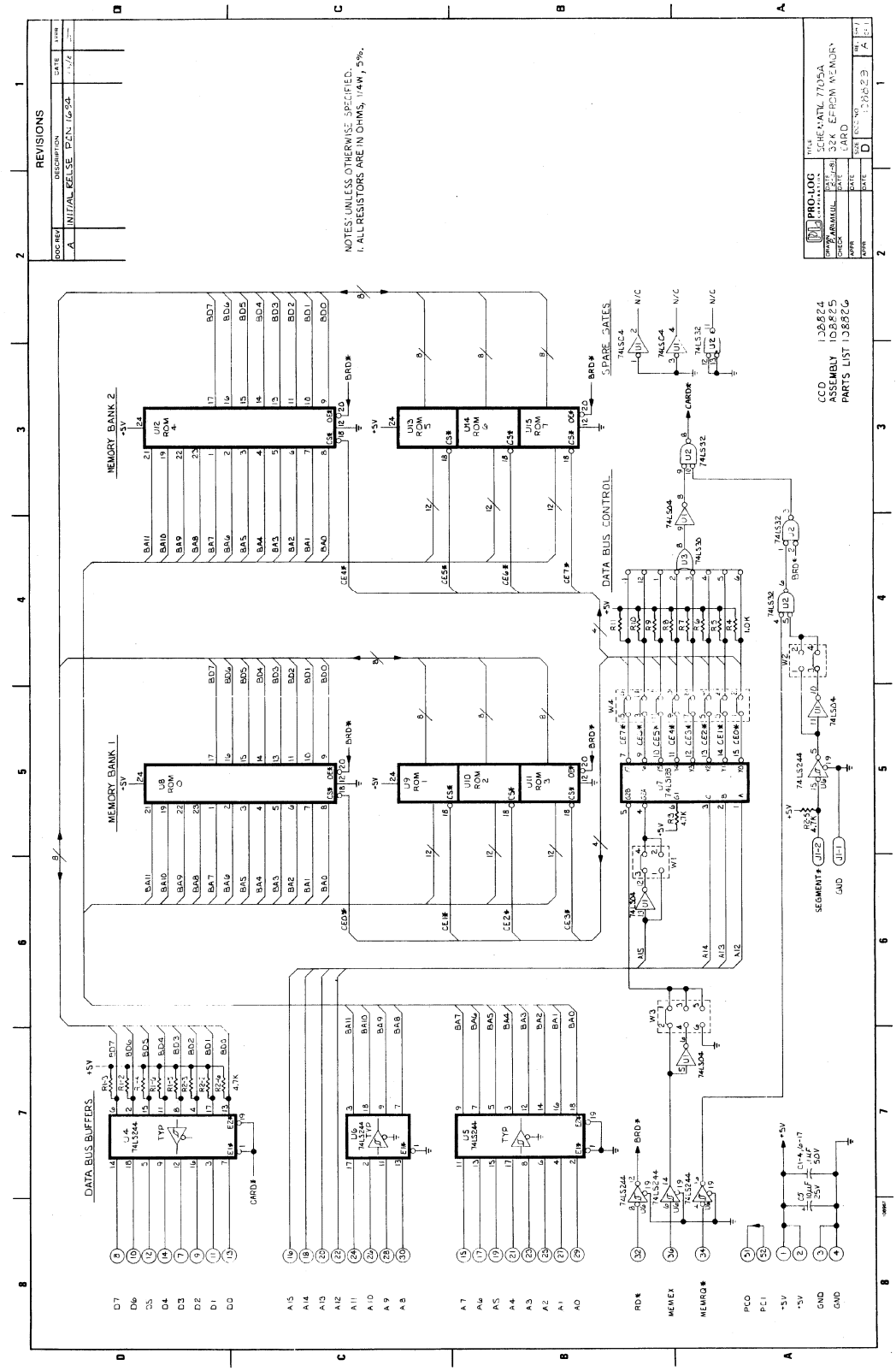


Figure 5-1. Schematic for 7705A 32K EPROM Memory Card

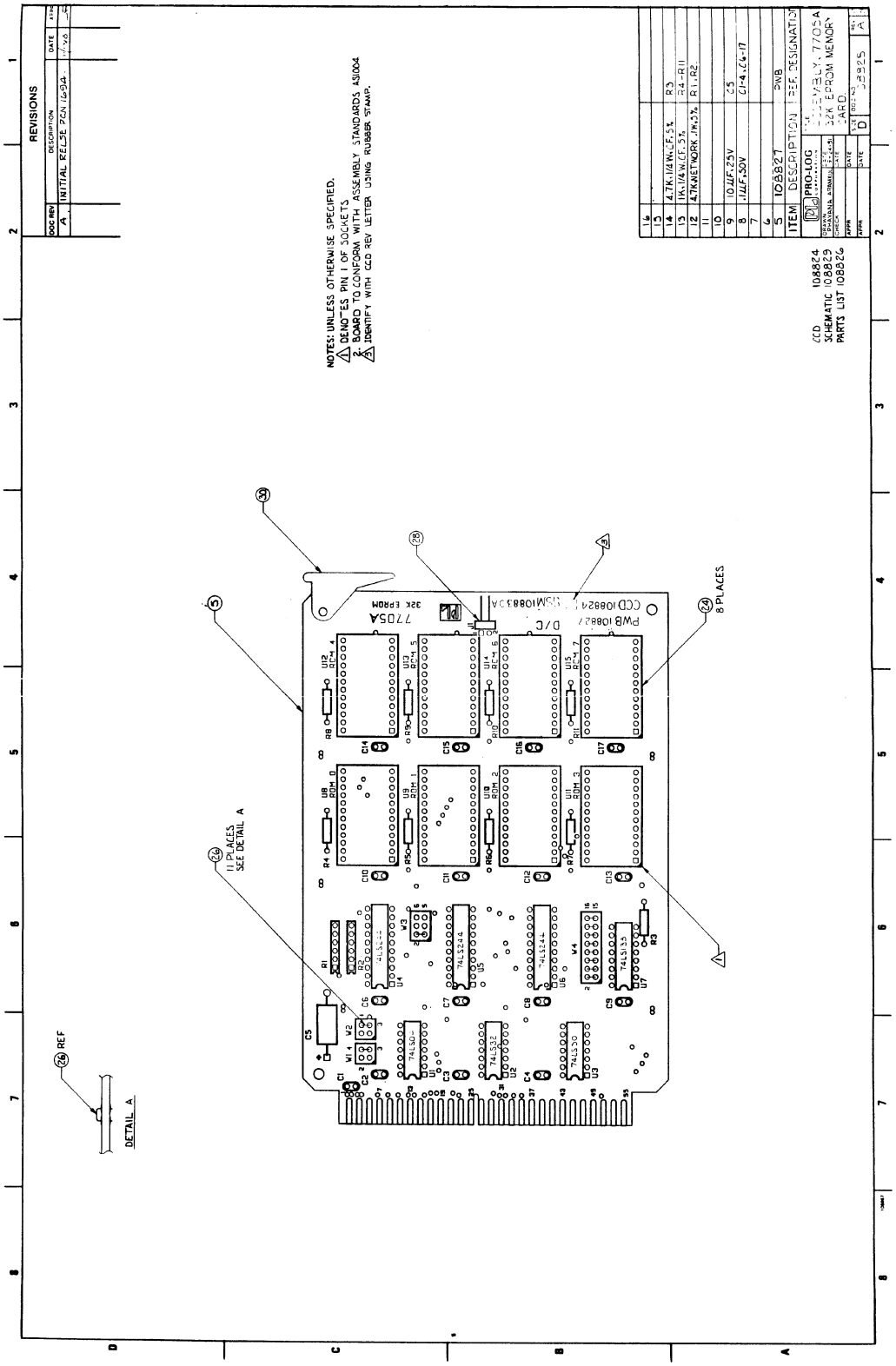


Figure 5-2. Assembly for 7705A 32K EPROM Memory Card

Operational Overview

Address Decoding

Address lines A0-A11 go through buffers U5 and one half of U6 and from there go directly to the EPROM sockets. See Figure 5-3, Address Decoding.

Address lines A12-A15 are decoded by U7 along with the MEMEX line. Address line A15 is inverted by U1 and then connects to U7 through Jumper W-1 position 3-4. This maps the card to addresses 8000-FFFF. Remapping the card to addresses 0000-7FFF is accomplished by removing jumper W1 from position 3-4 and replacing it with one at position 1-2. This bypasses the inverter and connects A15 directly to U7.

The MEMEX input to U7 is low-level active. If the input is tied to ground by placing a jumper at W3 position 5-6, the card will be permanently enabled and ignore MEMEX.

If MEMEX is controlled externally, the incoming signal can be either high-level active or low-level active. After being buffered by U6 the line can either be inverted by U1 or bypass the inverter. With the jumper W3 in position 3-4 the line is high-level active. With the jumper in position 1-2, as it is when the card is shipped, the line is low-level active.

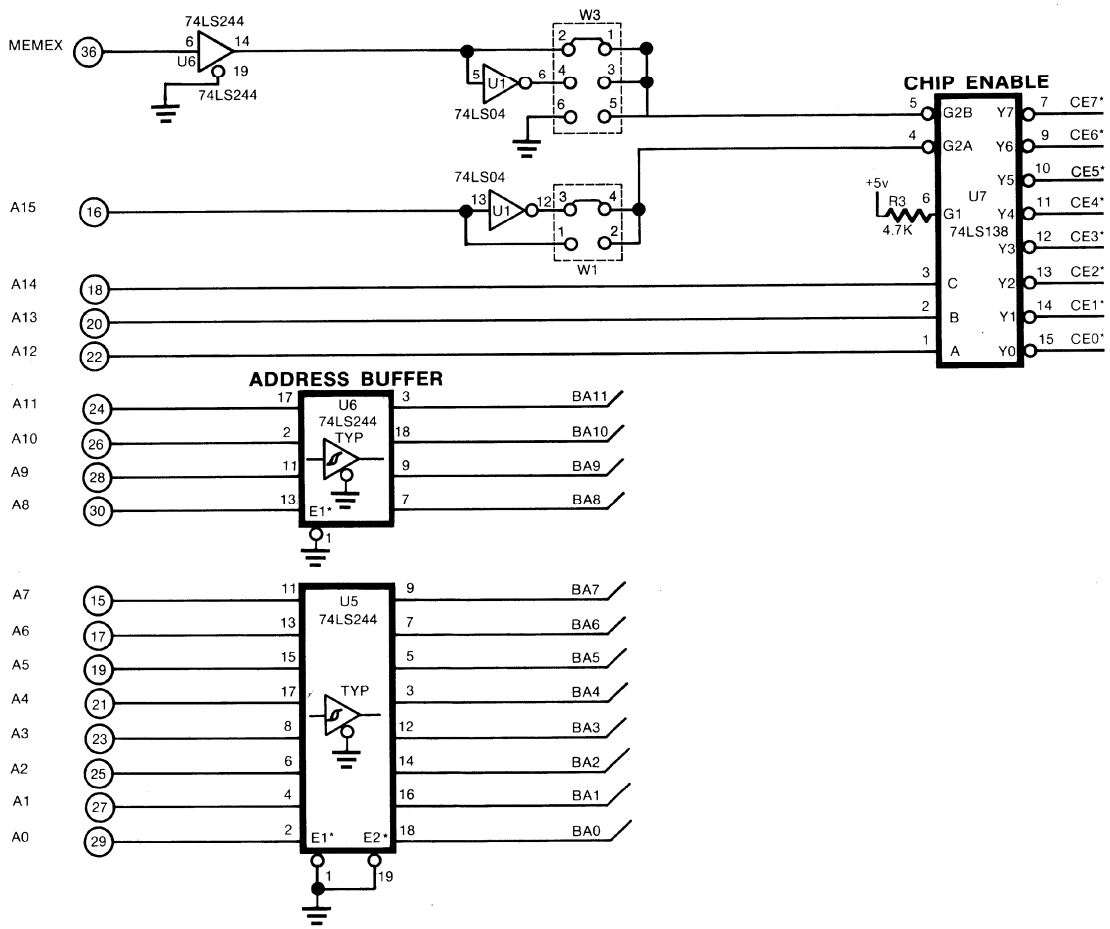


Figure 5-3. Address Decoding Circuit for 7705A.

Chip Enable

The Chip Enable signals CEO-CE7 are generated by address decoder U7 and go directly to the EPROM sockets, one to each socket. See Figure 5-4, Chip Enable. Any unused socket can be disabled by removing the correct jumper. Jumpers W4, position 1-2 through 15-16, correspond to sockets 0-7 respectively. Besides removing the chip enable signal from the socket, removing one of these jumpers also disables the data bus buffer over the address range of the unused socket. This is because the chip enable signals also go to OR gate U3. The resulting signal is part of the data bus buffer logic. If a chip enable jumper is removed, the data bus buffer does not get enabled. Note that there are pullup resistors on the Chip Enable lines to ensure that they stay in the inactive state if a jumper is removed.

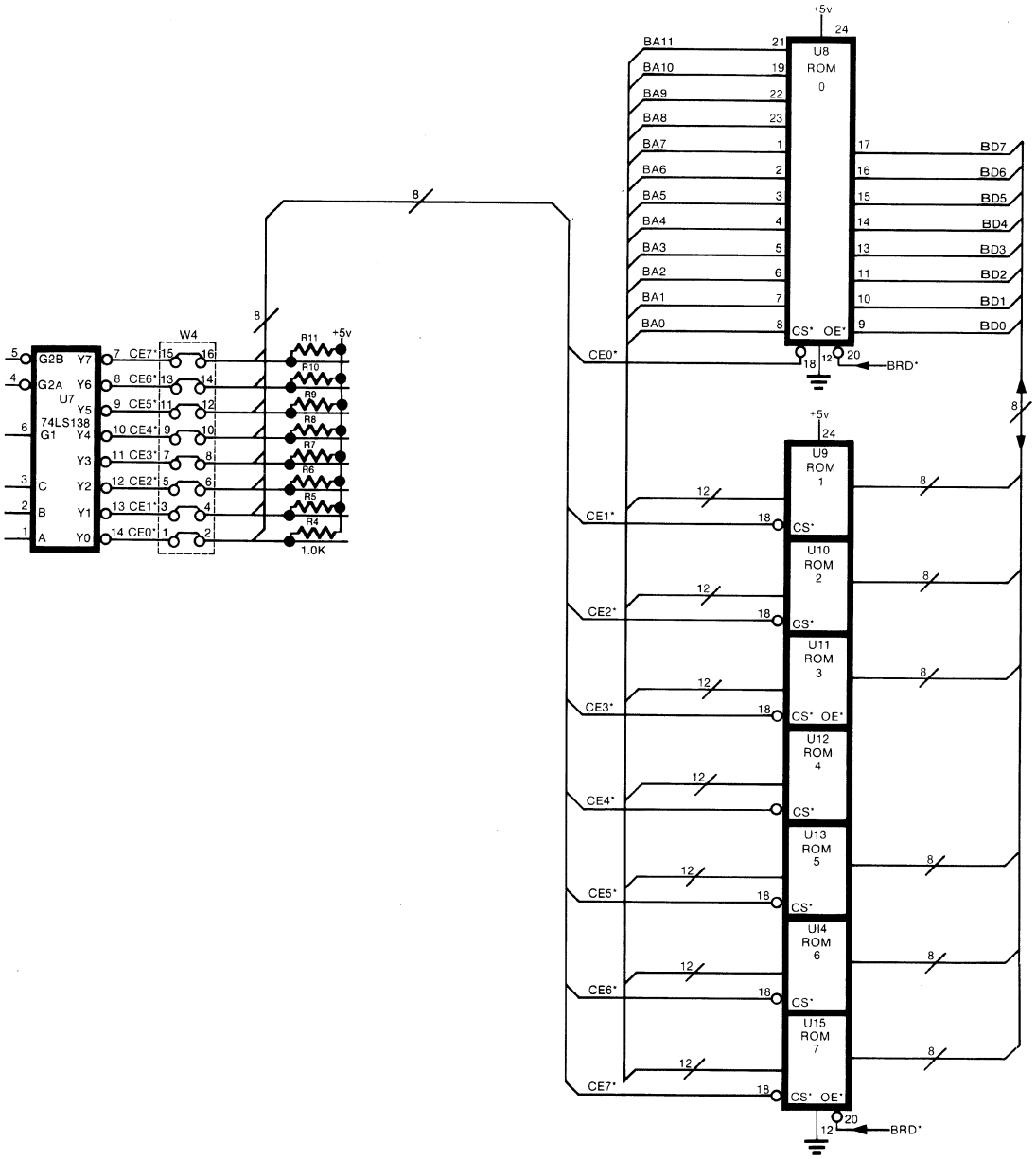


Figure 5-4. Chip Enable Circuit for 7705A.

Output Enable

The output enable signal required by 2732/2732A EPROMs is generated by the BRD* signal. See Fig.5-4, Chip Enable.

This signal is the STD BUS RD* signal after it has been buffered by U6.

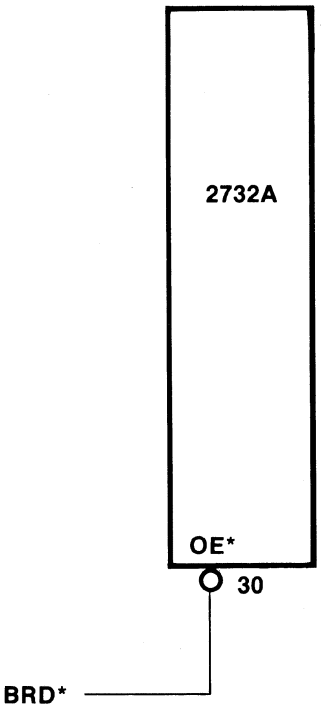


Figure 5-5. ROM Output Enable for 7705A.

Data Bus Buffer

The Data Bus Buffering is done by U4. See Figure 5-6, Data Bus Buffer. It is unidirectional, three-state, and non-inverting. The logic which controls the buffer enable signal is comprised of three gates from U2. The conditions that need to exist for the bus buffer to be enabled are as follows.

First of all, the output of OR gate U3 signal needs to be active. This is a function of the address lines, the MEMEX line, and the Chip Enable lines. The address lines and MEMEX line are explained in the Address Decoder section, and the Chip Enables are explained in the Chip Enable section.

Secondly, Segment Select must be active. Segment Select, after being buffered by U6, can be inverted or not inverted depending on the position of jumper W2. With the jumper in position 3-4, as it is when the card is shipped, Segment Select is high level active. With the jumper in position 1-2 it is low-level active. Note that there is a pull-up resistor on the line where it enters the card. This means that if the line is left unconnected, jumper W2 should be left in position 3-4 for the card to be enabled.

Thirdly, the BRD* signal needs to be active. This signal is also an output enable for the memory chips as described in the Output Enable section.

Fourthly, the MEMRQ* signal must be active. The MEMRQ* comes from the STD BUS and is buffered by U6.

When all of these conditions exist, the buffer is enabled out, otherwise it is left floating.

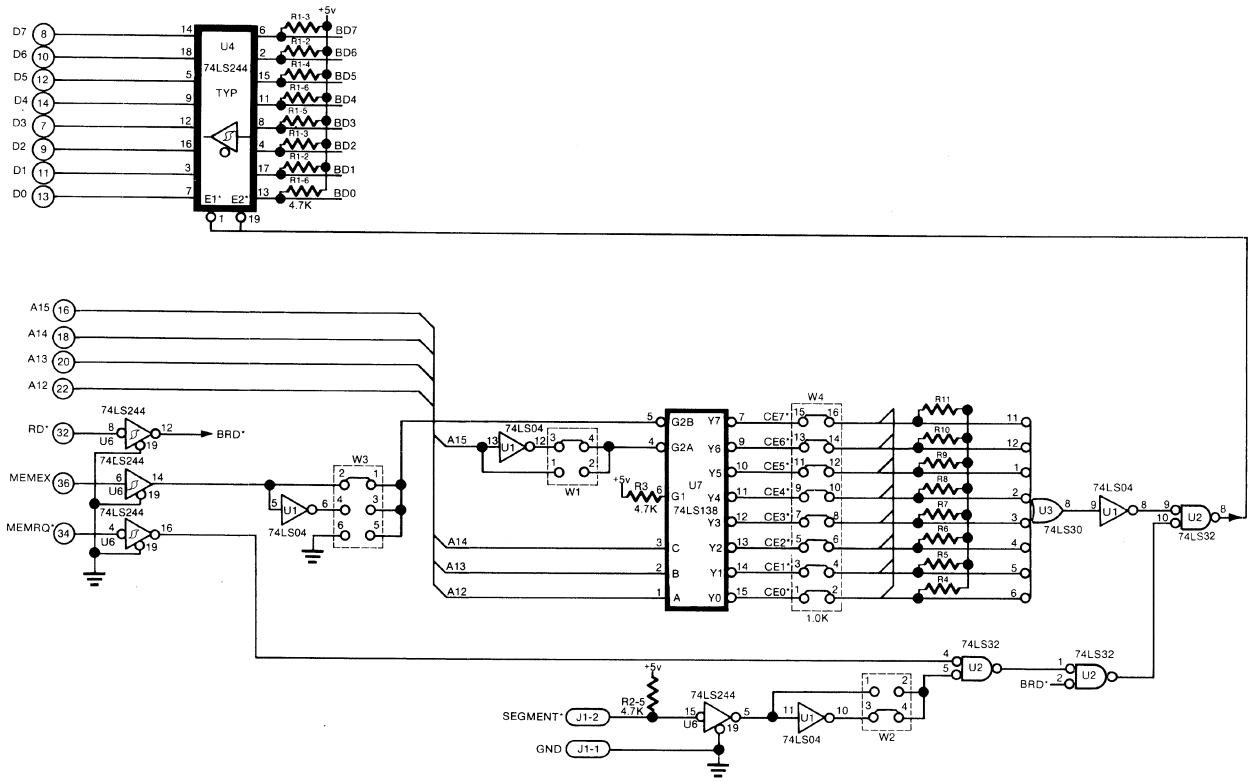


Figure 5-6. Data Bus Buffer Circuit for 7705A.

Return for Repair Procedures

Domestic Customers:

1. Call our factory direct at (408) 372-4593, and ask for CUSTOMER SERVICE.
2. Explain the problem and we may be able to solve it on the phone. If not, we will give you a Customer Return Order (CRO) number.

   Mark the CRO number on the shipping label, packing slip, and other paperwork accompanying the return. We cannot accept returns without a CRO.
3. Please be sure to enclose a packing slip with CRO number, serial number of the equipment and if applicable, reason for return, with the name and telephone number of the person we should contact (preferably the user), if we have any further questions.
4. Package the equipment in a solid cardboard box secured with packing material.

   CAUTION: Loose MOS integrated circuits, or any product containing CMOS integrated circuits, must be protected from electrostatic discharge during shipment. Use conductive foam pads or conductive plastic bags, and never place MOS or CMOS circuitry in contact with Styrofoam materials.
5. Ship prepaid and insured to:

   Pro-Log Corporation
   2411 Garden Road
   Monterey, Calif. 93940

   Reference CRO #_____

International Customers:

Equipment repair is handled by your local Pro-Log distributor. If you need to contact Pro-Log, the factory can be reached at any time by TWX at 910-360-7082.

Limited Warranty:

Seller warrants that the articles furnished hereunder are free from defects in material and workmanship and perform to applicable, published Pro-Log specifications for two years from date of shipment. This warranty is in lieu of any other warranty expressed or implied. In no event will Seller be liable for special or consequential damages as a result of any alleged breach of this warranty provision. This liability of Seller hereunder shall be limited to replacing or repairing, at its option, any defective units which are returned F.O.B. Seller's plant. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, unauthorized repair or installation are not covered by warranty. Seller shall have the right of final determination as to the existence and cause of defect. As to items repaired or replaced, the warranty shall continue in effect for the remainder of the warranty period, or for ninety (90) days following date of shipment by Seller or the repaired or replaced part whichever period is longer. No liability is assumed for expendable items such as lamps and fuses. No warranty is made with respect to custom equipment or products produced to Buyer's specifications except as specifically stated in writing by Seller and contained in the contract.